DRIVING A DRAM SENSE AMPLIFIER HAVING LOW THRESHOLD VOLTAGE PMOS TRANSISTORS

Abstract of the Disclosure

Circuits and methods for driving a DRAM sense amplifier having low threshold voltage PMOS transistors are presented. The source terminal of a low V_{tp} PMOS transistor is maintained at ground potential during DRAM standby mode. The source terminal of the low V_{tp} PMOS transistor is raised to an intermediate supply voltage responsive to a transition from DRAM standby mode to either DRAM read mode, write mode, or refresh mode and prior to development of a differential voltage between the gate and drain terminals of the low V_{tp} PMOS transistor. The circuits and methods of the invention advantageously limit current loss through the low V_{tp} PMOS transistor when the differential voltage develops between the gate and drain terminals of that low V_{tp} PMOS transistor and in the event of a word line and digital line short-circuit.